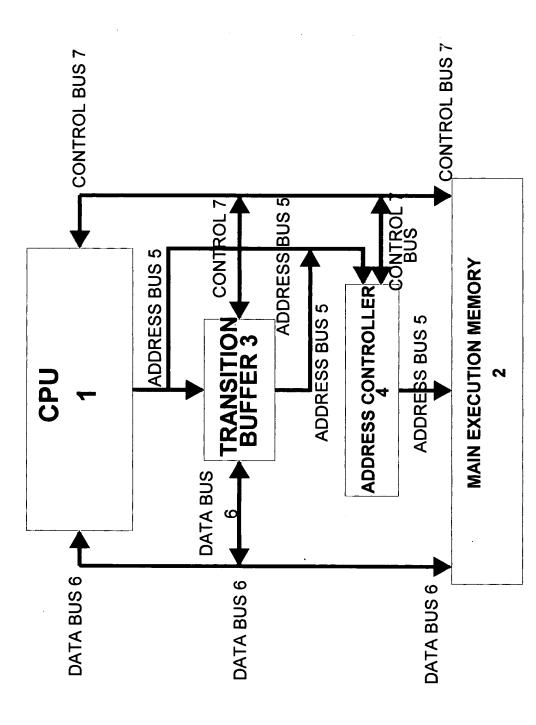
## 1 OF 12 SHEETS



ARCHITECTURAL REPRESENTATION OF CACHELESS COMPUTER SYSTEM FIGURE - 1

TOOP 12 SHEETSOT

FIGURE - 2

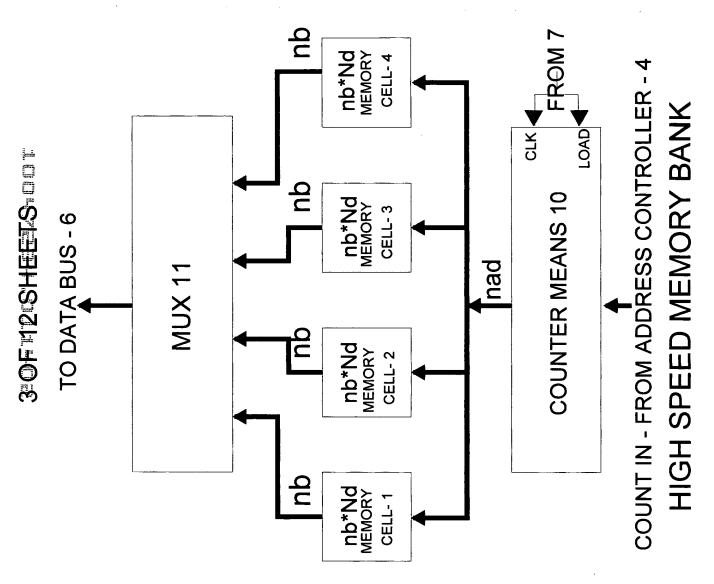
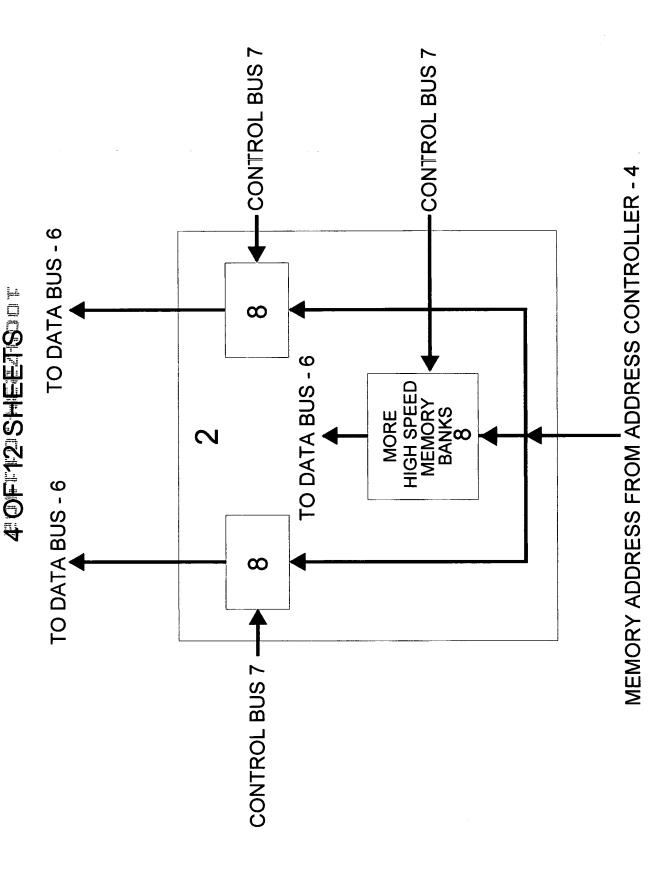
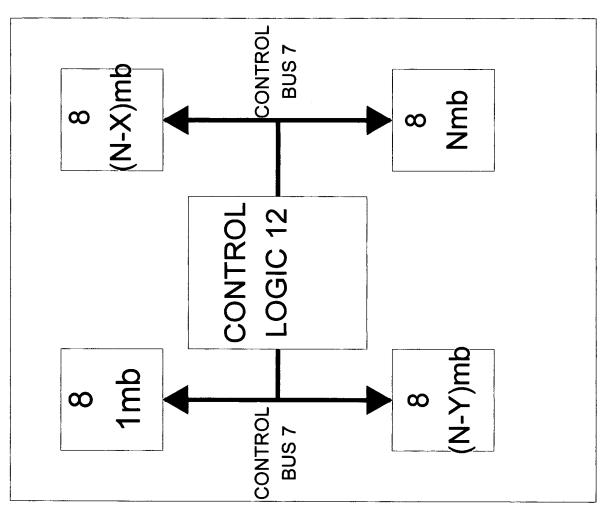


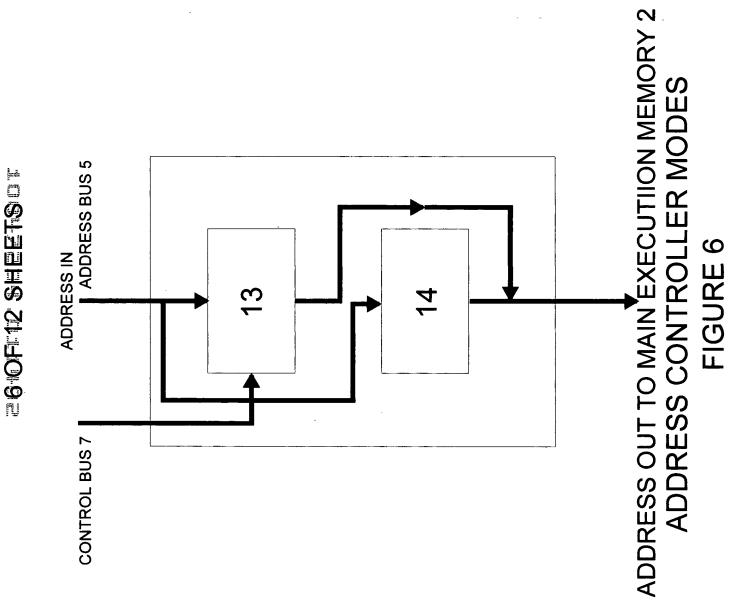
FIGURE 3



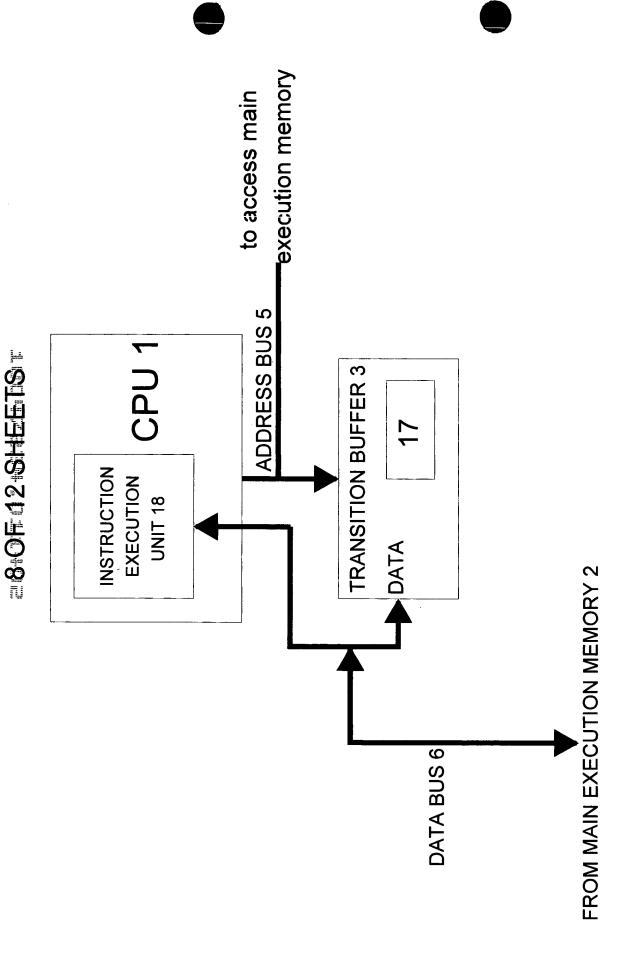
CONNECTION SCHEME FOR HIGH SPEED MEMORY BANKS FIGURE 4



FLEXIBLE CONNECTION SCHEME FOR MAIN EXECUTION MEMORY FIGURE 5



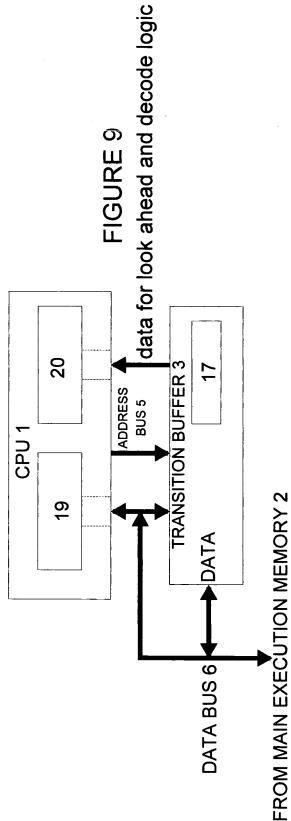
7 OF Y2 SHEPFS (+CIT



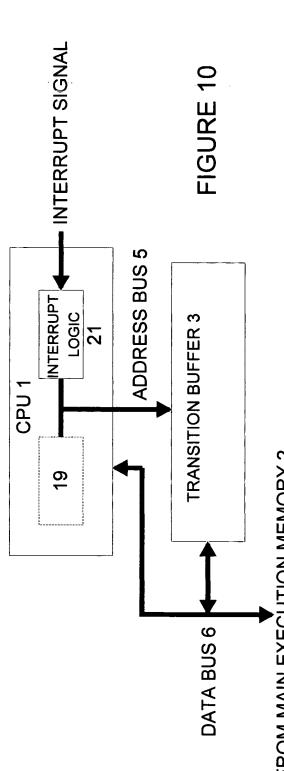
IMPLEMENTATION OF NON PIPELINED ARCHITECTURE

## FIGURE 8

## 9 OF A STEELS HOLF

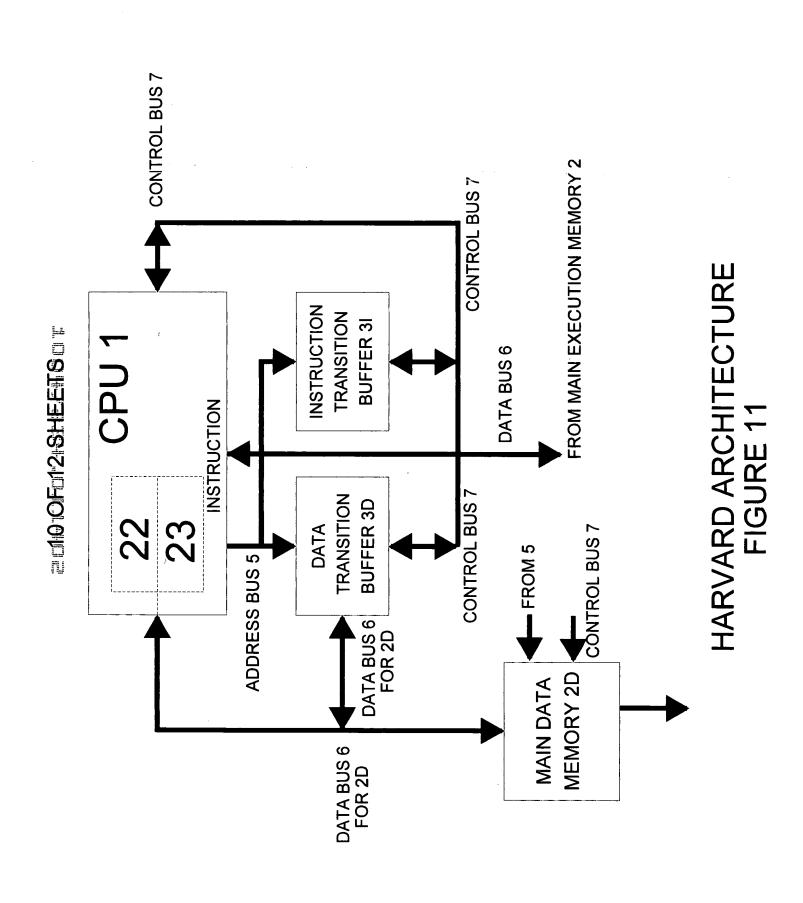


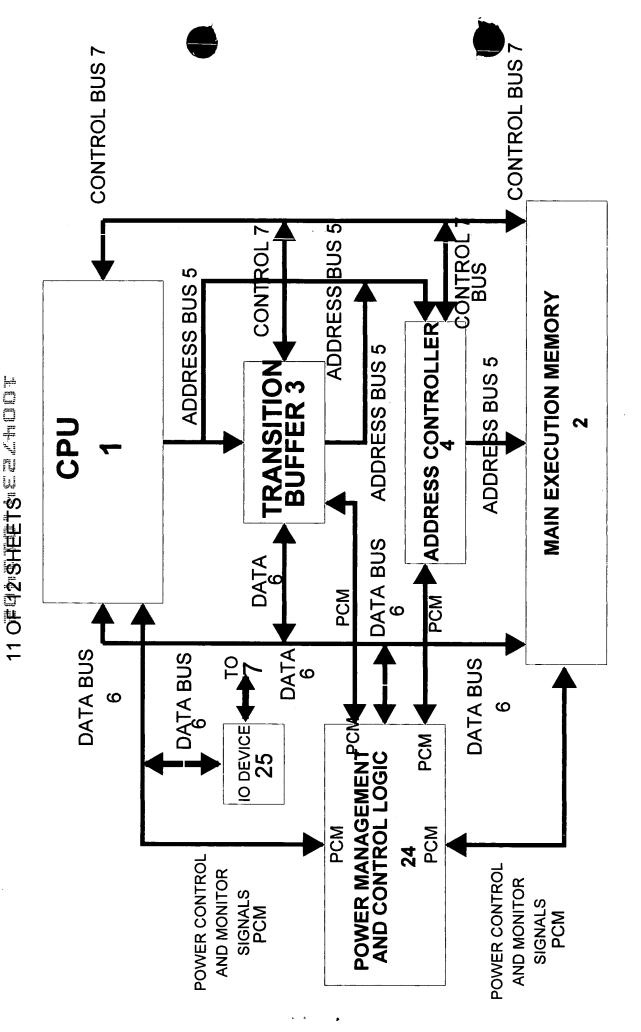
## IMPLEMENTATION OF PIPELINED ARCHITECTURE



FROM MAIN EXECUTION MEMORY 2

IMPLEMENTATION OF INTERRUPT LOGIC





POWER MANAGEMENT AND CONTROL LOGIC FIGURE 12

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**12 OF 12 SHEETS** 

PARALLEL OPERATION WITH MULTIPROCESSORS FIGURE 13

■ MAIN EXECUTION MEMORY 2

**CONTROL BUS 7** 

ADDRESS BUS 5

**CONTROL BUS 7** 

**ADDRESS CONTROLLER 4** 

ADDRESS BUS 5

DATA BUS 6